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EXAMINER	
VITAL, PIERRE M	
ART UNIT	PAPER NUMBER
2188	28

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/164,898	AKIYAMA, JAMES	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 September 2000* is: a)☒ approved b)☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed June 30, 2003 in response to PTO Office Action mailed February 27, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 19-37 have been presented for examination in this application. In response to the last Office Action, claims 19, 22, 25, 26, 29 and 35 have been amended. No claims have been canceled or added. As a result, claims 19-37 are now pending in this application.

3. The rejection of claims 19-37 under 35 USC 103 (a) is respectfully maintained and reiterated below for applicant's convenience.

Claim Objections

4. Claim 19 is objected to because of the following informalities:

In lines 9-10, the claim as amended recites "a second disk drive including second IDE electronics, said striping controller [coupled to said second IDE electronics] coupled to said striping controller".

It appears that applicant's amendment to the claim *inadvertently deleted* the recitation "coupled to said second IDE electronics" from the claim which now reads a "striping controller coupled to a striping controller".

Examiner would suggest amending the claim to *reinsert* the recitation --coupled to said second IDE electronics-- and *delete* --coupled to said striping controller--.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19, 21, 25-26, 28, 30 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (US5,694,581) and Jones et al. (US5,619,723) and further in view of Thompson et al (US6,341,342).

As per claims 19, 25, 28 and 35, Cheng discloses a system comprising: a Basic Input/Output System (BIOS) [col. 6, lines 4-6]; a system bus coupled to a BIOS [Col. 6, Lines 5-7]; an integrated drive electronics (IDE) interface coupled to a system bus that receives disk drive requests from said BIOS via said system bus [col. 5, line 46 - col. 6, Line 7; col. 6, lines 30-35].

However, Cheng fails to specifically teach a striping controller coupled to said IDE interface; a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics; and, a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics, a striping

controller connected between said first and second disk drives and said interface, said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel.

Thompson discloses a striping controller coupled to said IDE interface [Fig. 1B, *PCI-IDE adapter card 158*]; a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics; and a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics {*controller on same card as disk drives 124, 126;* controller 118 coupled to drives 124, 126} [Fig. 1B, col. 6, lines 35-55].

Jones discloses first and said second disk drives each having data separator electronics, data formatting electronics and head positioning electronics [Col.14, Lines 30-55]; said striping controller causing data being transmitted between said interface and said system bus and said first and second drives to be substantially read or written in parallel [Col.16, Lines 32-35].

It would have been obvious to one of ordinary skill in the art, having the teachings of Thompson and Jones and Cheng before him at the time the invention was made, to modify the system taught by Jones to include a striping controller connected between said first and second disk drives and said interface, said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel; an interface connected to the system bus and receiving requests from the BIOS via said system bus because it would have provided faster controller operation by (1) reducing the number of queued

commands that must be serviced by the array controller during disk drive operation [col. 3, lines 6-8, 24-25] as taught by Thompson and (2) increased information transfer speed by allowing parallel read/writes by the disk drives [col. 6, lines 7-9] as taught by Jones.

As per claims 21 and 30, Thompson discloses data being transmitted between the system bus and the first and second disk drives is subdivided into a plurality of sequential blocks [col. 1, lines 43-54].

As per claim 26, Thompson discloses receiving an IDE request at a striping controller [col. 7, lines 4-25].

7. Claims 20, 22, 27, 29, 31, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (US5,694,581) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and further in view of Anderson (US5,905,910).

As per claims 20, 22, 27, 29, 31, 34 and 36, the combination of Thompson and Jones and Cheng teach the claimed invention as detailed above in the previous paragraphs. However, neither Thompson nor Jones nor Cheng specifically teach interleaving data so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive; and the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining

blocks; and a control logic receives a system request intended for a single physical drive from the system bus as recited in the claims.

Anderson teaches interleaving data so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive [col.4, lines 16-30]; the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks [col.11, lines 35-50; col.12, lines 3-23]; a control logic receives a system request intended for a single physical drive from the system bus [Col.7, lines 60-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of Thompson and Jones and Cheng and Jenkins before him at the time the invention was made, to modify the system taught by Thompson and Jones and Cheng to include interleaving data so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive; and the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks; and a control logic receives a system request intended for a single physical drive from the system bus because it would have reduced disk access time and increased the efficiency of the system by allowing both disk drives to respond to commands that overlap in time [col. 12, lines 20-23] as taught by Anderson.

8. Claims 23, 24, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (US5,694,581) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and further in view of Jenkins (US4,047,157).

As per claims 23, 24, 32 and 33, the combination of Thompson and Jones and Cheng teach the claimed invention as detailed above in the previous paragraphs. However, neither Thompson nor Jones nor Cheng specifically teach that the system request includes a sector bit string, a head bit string, a track bit string and a driver bit; and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive as recited in the claims.

Jenkins teaches a controller for use in a data processing system wherein in the track/sector register 146 Track Address and Sector Address bit positions identify, respectively, the track and sector on a disk to be involved in a transfer; in a fixed-head unit, the Track Address bits identify a specific head [col. 20, lines 38-42]; a Write signal, produced in response to the function bits, enables drivers 297 to load data onto the data set 101 [col. 26, lines 26-28]; and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive [col. 20, lines 38-65].

It would have been obvious to one of ordinary skill in the art, having the teachings of Thompson and Jones and Cheng and Jenkins before him at the time the invention was made, to modify the system taught by Thompson and Jones and Cheng

to include sector bit string, head bit string, track bit string and driver bit in the system request and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive because it would have improved processing speeds and memory access times by providing the system identification information for the physical location on the drive from which the data file will be read or written [col. 2, lines 28-30] as taught by Jenkins.

9. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (US5,694,581) and Jones et al. (US5,619,723) and further in view of Thompson et al (US6,341,342) and Mizuno et al (US5,608,891).

As per claim 37, the combination of Thompson and Jones and Cheng teach the claimed invention as detailed above in the previous paragraphs. However, neither Thompson nor Jones nor Cheng specifically teach a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device as recited in the claims.

Mizuno discloses a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory

coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device [col. 17, lines 8-28].

It would have been obvious to one of ordinary skill in the art, having the teachings of Thompson and Jones and Cheng and Mizuno before him at the time the invention was made, to modify the system taught by Thompson and Jones and Chen to include a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device because it would have improved system performance by reducing the time required for temporarily storing write data in memory and then exclusive Oring the data to find redundant data [col. 18, lines 46-53] as taught by Mizuno.

Response to Arguments

10. Applicant's arguments filed June 30, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

The prior art of record does not teach or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that Cheng discloses a system bus (*i.e., ISA bus 135*) coupled to an IDE interface (*i.e., IDE interface 110*). It should be borne in mind that, in

discussions of electrical components, the terms "connected", "operatively connected", "electrically connected", and like terms denote an electrical path between two components. It is understood, however, that such terms do not preclude the existence of additional components interposed between the two original components, even if an additional such component has the capability of interrupting or affecting signal or data transmission between the two original components. Only through the use of the term "directly connected", or like terms, is it intended to denote an electrical connection between two components that precludes any additional components, other than an electrical conductor, interposed between the two original components.

Cheng further discloses an IDE interface that receives disk drive requests from a BIOS via the system bus as detailed in column 6, lines 4-35 and Fig. 1. The BIOS 140 is coupled to the ISA bus 135, which is employed as an I/O bus, i.e., system bus (*see column 6, lines 4-10*). Furthermore, Cheng discloses that read/write request from the BIOS 140 is received from the ISA bus 135 (*see column 6, lines 34-35*).

Thus, it can be clearly seen that Cheng discloses an IDE interface coupled to a system bus (*IDE interface 110 coupled to ISA bus 135*) that receives disk drive requests from a BIOS via the system bus (*BIOS receives read/write requests from ISA bus 135*).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Pierre M. Vital
July 29, 2003

REGINALD G. BRAGDON
PRIMARY EXAMINER